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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,804	09/12/2006	Takumi Katoh	40404.59/ko	1574

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
10/06/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/598,804	KATOH ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/12/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/598804 Attorney's Docket #: 40404.59/ko
Filing Date: 9/12/2006; claimed foreign priority to 3/12/2004

Applicant: Katoh et al.

Examiner: Alexander Williams

This application is a 371 of a PCT/JP05/04337 filed 3/11/2005.

Applicant's Pre-Amendment filed 9/12/2006 has been acknowledged.

Claims 1-8 have been cancelled.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 9-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Matsumoto (U.S. Patent Application Publication # 2004/0207079 A1).

9. Matsumoto (figures 1 to 9) specifically figure 3 show a semiconductor device comprising: at least a first and a second power source system, the first and second power source systems each including: a power supply bonding pad **11**, a ground bonding pad **12**, and at least one signal bonding pad **13,14** arranged on a semiconductor substrate; an I/O circuit **2** that is connected to

each of the power supply bonding pad, the ground bonding pad and the at least one signal bonding pad, and arranged to input or output a signal from or to the signal bonding pad; and a first ESD protective bonding pad **21** and a signal ESD protective element section **(ESD)** connected to the signal bonding pad and the first ESD protective bonding pad; wherein the first ESD protective bonding pads of the first and second power source systems are connected to one another.

10. The semiconductor device according to claim 9, Matsumoto further comprising a power source ESD protective element section connected to either of the first ESD protective bonding pads of the first and second power source systems.

11. The semiconductor device according to claim 9, Matsumoto show wherein each of the first and second power source systems further comprises a power supply terminal connected to the power supply bonding pad, a ground terminal connected to the ground bonding pad, and a signal terminal connected to the signal bonding pad; wherein, in each of the first and second power source systems, the first ESD protective bonding pad is connected to one of the power supply terminal and the ground terminal.

12. The semiconductor device according to claim 11, Matsumoto show wherein, in each of the first and second power source systems, the connection between the power supply bonding pad and the power supply terminal, the connection between the ground bonding pad and the ground terminal, the connection between the signal bonding pad and the signal terminal, and the connection

between the first ESD protective bonding pad and one of the power supply terminal and the ground terminal, are via bonding wire.

13. The semiconductor device according to claim 9, Matsumoto show wherein each of the first and second power source systems further comprises, on the semiconductor substrate, a second ESD protective bonding pad connected to the signal ESD protective element section, and the second ESD protective bonding pads of the first and second power source systems are connected to one another.

14. The semiconductor device according to claim 13, Matsumoto further comprising a power source ESD protective element section connected to either of the first ESD protective bonding pads and to either of the second ESD protective bonding pads of the first and second power source systems.

15. The semiconductor device according to claim 14, Matsumoto show wherein each of the first and second power source systems further comprises: a power supply terminal connected to the power supply bonding pad, a ground terminal connected to the ground bonding pad, and a signal terminal connected to the signal bonding pad; wherein in each of the first and second power source systems, the first ESD protective bonding pad is connected to one of the power supply terminal and the ground terminal, and the second ESD protective bonding pad is connected to the other of the power supply terminal and the ground terminal.

16. The semiconductor device according to claim 15, Matsumoto show wherein, in each of the first and second power source systems, the connection between the power supply bonding pad and the power supply terminal, the connection between the ground bonding pad and the ground terminal, the connection between the signal bonding pad and the signal terminal, the connection between the first ESD protective bonding pad and one of the power supply terminal and the ground terminal, and the connection between the second ESD protective bonding pad and the other of the power supply terminal and the ground terminal, are via bonding wire.

17. The semiconductor device according to claim 13, Matsumoto show wherein each of the first and second power source systems further comprises: a power supply terminal connected to the power supply bonding pad, a ground terminal connected to the ground bonding pad, and a signal terminal connected to the signal bonding pad; wherein in each of the first and second power source systems, the first ESD protective bonding pad is connected to one of the power supply terminal and the ground terminal, and the second ESD protective bonding pad is connected to the other of the power supply terminal and the ground terminal.

18. The semiconductor device according to claim 17, Matsumoto show wherein, in each of the first and second power source systems, the connection between the power supply bonding pad and the power supply terminal, the connection between the ground bonding pad and the ground terminal, the connection between the signal bonding pad and the signal terminal, the connection

between the first ESD protective bonding pad and one of the power supply terminal and the ground terminal, and the connection between the second ESD protective bonding pad and the other of the power supply terminal and the ground terminal, are via bonding wire.

19. The semiconductor device according to claim 10, Matsumoto show wherein each of the first and second power source systems further comprises a power supply terminal connected to the power supply bonding pad, a ground terminal connected to the ground bonding pad, and a signal terminal connected to the signal bonding pad; wherein, in each of the first and second power source systems, the first ESD protective bonding pad is connected to one of the power supply terminal and the ground terminal.

20. The semiconductor device according to claim 19, Matsumoto show wherein, in each of the first and second power source systems, the connection between the power supply bonding pad and the power supply terminal, the connection between the ground bonding pad and the ground terminal, the connection between the signal bonding pad and the signal terminal, and the connection between the first ESD protective bonding pad and one of the power supply terminal and the ground terminal, are via bonding wire.

The listed references are cited as of interest to this application., but not applied at this time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

10/4/2008

/Alexander O Williams/
Primary Examiner, Art Unit 2826